

ABSTRACT

The present invention provides a content addressable memory (CAM) match detection circuit that maintains traditionally achieved levels of accuracy while greatly reducing the amount of power dissipated. In accordance with an exemplary embodiment of the invention, rather than allowing the Matchline voltage to swing between a precharge voltage level (e.g., VDD) and Ground, the Matchline voltage is restricted to swinging between the precharge voltage level (e.g., VDD) and a Negative Reference voltage level that is lower than the precharge voltage level but higher than Ground.